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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EDWIN FRANKLIN BARRY and
GERALD GEORGE PECHANEK

Appeal 2009-005669
Application 10/815,294
Technology Center 2100

Before: HOWARD B. BLANKENSHIP, JOHN A. JEFFERY, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

STEPHENS, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

Appellants appeal under 35 U.S.C. § 134(a) (2002) from a final rejection of claims 1-19. We have jurisdiction under 35 U.S.C. § 6(b) (2010).

We AFFIRM-IN-PART.

Introduction

According to Appellants, the invention is a system and method for improving signal processing systems through techniques for instruction execution that include translating storage device addresses prior to data access (Spec. 1, Field of the Invention). The invention is directed toward efficient reordering of data and for performing data exchanges within a register file or memory (Spec. 2, ll. 8-11).

STATEMENT OF CASE

Exemplary Claim(s)

Claim 1 is an exemplary claim and is reproduced below:

> 1. A processor address translation apparatus for translating an instruction operand address to a different operand address, the processor address translation apparatus comprising:
>
> a memory with an address input for selecting a data element from a plurality of data elements;
>
> an instruction register for receiving an instruction encoded with an operand address in an operand address bit field of the instruction and control information indicating the operand address is to be translated as part of the instruction's execution; and

> an address translation unit for accessing the memory in a translation pattern, having the operand address bit field as input and, in response to the instruction received in the instruction register, directly translating the operand address bit field received as input to form the different operand address in accordance with the translation pattern, the different operand address accessing a data element film the memory through the address input.

Prior Art

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Pechanek	US 6,173,389 B1	Jan. 9, 2001
Choquette	US 2002/0199084 A1	Dec. 26, 2002
Dowling	US 6,823,505 B1	Nov. 23, 2004
Nair	US 6,944,747 B2	Sep. 13, 2005

"*Pentium Processor Family Developer's Manual*", Volume 3: Architecture and Programming Manual, 1995. (Hereinafter "Intel")

TM320 Second-Generation Digital Signal Processors, Nov. 1990.

REJECTIONS

Claims 1, 2, 4-6, 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dowling and Intel. (Ans. 4).

Claims 3 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dowling, Intel, and Nair. (Ans. 7).

Claims 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dowling and Nair. (Ans. 8).

Claims 7-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pechanek and Dowling. (Ans. 10).

Claims 11-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dowling and Choquette. (Ans. 13).

Claims 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dowling, Choquette, and Nair. (Ans. 16).

GROUPING OF CLAIMS

(1) Appellants argue claims 1, 2, 4-6, 16, and 17 as a group on the basis of claim 1 (App. Br. 16-19). We select independent claim 1 as the representative claim. We will, therefore, treat claims 2, 4-6, 16, and 17 as standing or falling with representative claim 1.

(2) Appellants argue claims 3 and 19 as a group on the basis of claim 3 (*id.* at 19-21). We accept dependent claim 3 as the representative claim. We will, therefore, treat claim 19 as standing or falling with representative claim 3.

(3) Appellants argue independent claim 18 separately (*id.* at 21-23). We will consider claim 18 separately.

(4) Appellants argue claims 7-10 as a group on the basis of independent claim 7 (*id.* at 23-24). We accept claim 7 as the representative claim. We will, therefore, treat claims 8-10 as standing or falling with representative claim 7.

(5) Appellants argue claims 11-14 as a group on the basis of claim 11 (*id.* at 24-26). We accept independent claim 11 as the representative claim. We will, therefore, treat claims 12-14 as standing or falling with representative claim 11.

(6) Appellants argue claim 15 separately (*id.* at 26-27). Accordingly, we will consider claim 15 separately.

We accept Appellants' grouping of the claims. *See* 37 C.F.R. § 41.37(c)(1)(vii). Arguments that Appellants could have made but chose not to make in the Briefs are deemed to have been waived. (*See In re Watts*, 354 F.3d 1362, 1368 (Fed. Cir. 2004)). Arguments not made by Appellants in the Briefs are waived. (*See* 37 C.F.R. § 41.37(c)(1)(vii) (2008)).

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ISSUE 1

35 U.S.C. § 103(a): claims 1, 2-6, 16, 17 and 19

Claims 1, 2, 4-6, 16, and 17

Appellants argue their invention is not obvious over Dowling and Intel because the combination does not teach

> an instruction register for receiving an instruction encoded with an operand address in an operand address bit field of the instruction and control information indicating the operand address is to be translated as part of the instruction's execution

and

> directly translating the operand address bit field received as input

as recited in claim 1. (App. Br. 16-18). More specifically, Appellants contend that Dowling does not transform the bit field which specifies the address registers (App. Br. 17). Instead, Appellants argue Dowling transforms the contents of the selected address register (*id.*). Dowling, according to Appellants, does not show a direct addressing path from an instruction register that receives an instruction (App. Br. 18).

Additionally, Appellants argue Intel does not teach a direct addressing format, but rather generation of an effective address by adding the disp16 value to an index value (App. Br. 17).

In response, the Examiner maintains that Dowling teaches the recited invention (Ans. 17). More specifically, the Examiner states that Dowling teaches translating the operand address through use of the programmable AAU (Ans. 19 and 21). The Examiner further maintains Appellants are arguing limitations not recited in the claim (Ans. 20).

Issue 1: Has the Examiner erred in finding that the combination of Dowling and Intel teaches or suggests "an instruction register for receiving an instruction encoded with an operand address in an operand address bit field of the instruction and control information indicating the operand address is to be translated as part of the instruction's execution" and "directly translating the operand address bit field received as input" as recited in claim 1?

FINDINGS OF FACT (FF)

Dowling

(1) Dowling describes a processor with programmable addressing modes that uses a programmable address arithmetic unit. The arithmetic unit comprises a programmable logic array or other programmable device coupled to address registers and the instruction stream. The arithmetic unit responds to instructions from the processor's instruction set. A first set of instructions controls initialization and configuration of the arithmetic unit

logic and the second set references operands using addressing mode(s) that calculate the operand's effective address using logic that has been programmed by the first set of instructions. (Abstract).

(2) The programmable AAU can programmably permutate bits in a 16-bit word. "This function is useful for generating addresses in a matrix when performing matrix arithmetic." (Col. 10, ll. 13-27).

(3) A matrix "A" 400 has sixteen elements arranged in four rows and four columns. Each element of the matrix A is denoted A(0,0), A (0, 1)…A(i, j)…A (3, 3), where the "i" index indicates the row and the "j" index indicates the column. (Col. 10, ll. 28-32 and Fig. 4A).

(4) Interchanging elements within the matrix is a common function in computer programs handling matrices. A common interchange is a transpose interchanging A(i,j) with A(j,i). Typically, a programmer that needs to transpose elements will generate the address of one element to be transposed and use that address to compute the address of the transposed element. (col. 10, ll. 50-58).

(5) Table 5 lists the code that performs a swap operation on a TMS320C2x with an added programmable AAU 350.

TABLE 5

Sample code to swap matrix elements in a DSP with programmable address unit

	Cycles	Code		
1.	1	LAR	AR4, *++	; AR4 = a (i, j), and transpose the address
2.	1	LAR	AR5, *++	; AR5 = a (j, i), and transpose the address
3.	1	SAR	AR5, *++	; a (i, j) = AR5, transpose the address
4.	1	SAR	AR4, *++	; a (j, i) = AR4, transpose the address

The "*++" instructs the processor to use the programmable AAU 350 to indicate auto-increment addressing. Assuming the program registers PRO-PR3 are loaded properly, the programmable AAU 350 will compute the transpose address. The code in Table 5 uses three registers: one to hold the addresses and two to hold the data. On each instruction, the address in the register is converted into the address of the corresponding transpose element. (Col. 13, ll. 19-49).

(6) The instruction "LAR: DEST:, TEMP" performs a "load mirrored address to destination" (col. 12, Table 2, cycle 25).

Dictionary

(7) The term "translate" means "to bear, remove, or change from one place, state, form, or appearance to another." *Merriam-Webster's Collegiate Dictionary* 1250 (10th ed. 2000).

(8) The term "directly" means "in a direct manner," "without delay," and "in a little while." *Merriam-Webster's Collegiate Dictionary* 327 (10th ed. 2000).

ANALYSIS

"an instruction register"

Appellants recite "an instruction register for receiving an instruction encoded with an operand address in an operand address bit field of the instruction and control information indicating the operand address is to be translated as part of the instruction's execution" in claim 1. The Examiner finds Dowling illustrates this limitation (FF 5). As illustrated in

Table 5, code is received that directs execution of a swap of matrix elements (FF 5).

"In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art." *Brookhill-Wilk 1, LLC. v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298 (Fed. Cir. 2003). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted).

Initially, we find transposing is "translating," when read broadly, but reasonably, transposing is changing an address from one address to another (changing from one state to another) (FF 7).

We find Dowling teaches an instruction to load the mirrored address to the destination (load the address from the mirrored address (using the programmable AAU 350) into the destination AR4) (FF 5 and 6). The Examiner finds the control information is the new "*++" notation indicating address translation (Ans. 4 and 5).

We are unclear (i) whether the Examiner is indicating the "*++" is the control information indicating the operand address is to be translated, or (ii) whether it is the operand address itself with the LAR instruction inherently having control information that indicates the mirrored address is to be translated to the destination. In case (i) then, it is unclear what the operand address would then be in the instruction shown in Table 5. Understanding the Examiner's mapping would require speculation on our part. We refuse to engage in speculation. The cited Intel reference does not cure the deficiencies of Dowling. Therefore, we are constrained to find the Examiner

has not shown "an instruction register for receiving an instruction encoded with an operand address in an operand address bit field of the instruction and control information indicating the operand address is to be translated as part of the instruction's execution"

"directly translating the operand address bit field received"

Appellants' arguments regarding direct and indirect addressing (App. Br. 17 and 18 and Reply Br. 2 and 3) are not persuasive as the claim recites "directly translating" (claim 1) or "translating directly" (claim 16) not "direct addressing." Thus, Appellants have not shown the Examiner erred in finding Dowling teaches "directly translating the operand address bit field received.

In light of our findings, we are constrained to find the Examiner has not shown Dowling teaches the invention as recited in claim 1 and commensurately recited in claim 16. Claims 2, 4-6 and 17 depend from claims 1 and 16, respectively, and were rejected under the same references.

Claims 3 and 19

Claims 3 and 19 which also depend from claims 1 and 16, respectively, were rejected under Dowling, Intel and Nair. The Examiner has not shown Nair cures the deficiencies of Dowling.

Thus, we conclude claims 1-6, 16, 17, and 19 have not been shown to be obvious over the cited prior art.

ISSUE 2

35 U.S.C. § 103(a): claim 18

Appellants assert their invention is not obvious over Dowling and Nair because the combination of references do not teach an address translation parameter control register located in the address translation memory or an address translation unit located in the address translation memory for translation as recited in claim 18. (App. Br. 21-23).

Specifically, Appellants contend that Dowling's data memory 120 is not an "address translation memory" having an "address translation parameter control register" or having an "address translation unit" but is instead a separate memory (App. Br. 22 and Reply Br. 6 and 7). Appellants argue the Specification provided a definition in the original claim 11 recitation of "an address translation memory device" (Reply Br. 5).

Appellants also argue Dowling performs the translating step before any read operation to the data memory 120 occurs in contrast to the recited read operation occurring before the translating step (App. Br. 23 and Reply Br. 7 and 8).

The Examiner finds Appellants have not defined "address translation memory" in their Specification and thus this memory can be reasonably interpreted as a memory device with logic and storage (Ans. 24). The Examiner also finds Dowling teaches the sequence of reads as recited (Ans. 29).

Issue 2: Has the Examiner erred in concluding that the combination of Dowling and Nair teaches loading a set of bits into an address translation

parameter control register located in the address translation memory; and enabling an address translation unit located in the address translation memory for translation?

FURTHER FINDINGS OF FACT (FF)

Dowling

(9) A register set 102 is comprised of address registers AR0, AR1,…ARn which provide data to the input of the AAU 150 (Fig. 2).

(10) The data memory 120 receives address input from a multiplexer 122 and stores program data (col. 8, ll. 14 and 15 and Fig. 2). The data memory is provided with a bi-directional data path to the data bus 112 (col. 7, ll. 58 and 59).

(11) The programmable AAU is programmed by loading data into programmable registers. The bits of the register determine which bit in an input word is mapped to a bit in the output word. (Col. 9, ll. 54 - col. 10, l. 3).

ANALYSIS

Appellants have not supplied an explicit definition for "address translation memory" "address translation parameter control register," or "address translation unit." Appellants reliance on claim 11 which recites an embodiment of an "address translation memory" is not a definition, but instead an example of what that memory may comprise. Nor do the portions of their Specification that Appellants point to support their assertion regarding the definition of "the address translation memory" (*See* App. Br. 22-23). These portions of the Specification describe "[a]nother aspect of the present invention" and an "exemplary storage subsystem" (Spec. 21-22).

They do not provide a definition. Moreover, Appellants' recitation of the address translation memory as including an address translation parameter control register and an address translation unit for translation, indicates the "memory" includes elements that do more than store. Therefore, we take a broad but reasonable definition of "address translation memory" and determine such a "memory" may encompass several of the elements disclosed by Dowling.

For example, the "address translation memory" recited by Appellants includes an address translation unit for translation. As discussed above in Issue 1, "translation" means to change from one state to another. We therefore find that the AAU 212 translates the first address to the second address as the matrix operation changes one address to another (FF 5). Thus, we find the element 150 of Dowling which includes a programmable AAU 212 is an address translation unit for translating and is part of the "address translation unit." We also find this element includes an address translation parameter control register as the program registers PRO – PR3 control parameters related to the address translation (FF 11).

Thus, we find Dowling teaches the recited "address translation memory."

Appellants' additional arguments regarding the order of the "initiating" and "translating" steps is unpersuasive. Unless the steps of a method actually recite an order, the steps are not ordinarily construed to require one. *Interactive Gift Express, Inc. v. CompuServe, Inc.*, 256 F.3d 1323, 1342 (Fed. Cir. 2001). *See also Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1369-71 (Fed. Cir. 2003) (district court erred in claim

construction by reading a step order from the written description into the claims).

Accordingly, based on the record before us, Appellants have not shown the Examiner erred in finding the combination of Dowling and Nair teach the invention as recited in claim 18. Thus, Appellants have not shown the Examiner erred in rejecting claim 18 under 35 U.S.C. § 103(a) for obviousness over Dowling and Nair.

ISSUE 3

35 U.S.C. § 103(a): claims 7-10

Appellants assert their invention is not obvious over Pechanek and Dowling because the combination of references do not disclose the logic to translate the operand address of a sequence of instructions to an RFI sequence of different operand addresses as recited in claim 7 (App. Br. 23-24).

ANALYSIS

For the reasons set forth above with respect to claim 1, in Issue 1, we are constrained to find the Examiner has not shown Dowling teaches "an instruction register for receiving an instruction encoded with an operand address and control information indicating the operand address is to be translated as part of the instruction's execution" as recited in claim 7. We also find the Examiner has not shown that Pechanek cures this deficiency. Accordingly, Appellants have shown the Examiner erred in rejecting claims 7-10 under 35 U.S.C. § 103(a) for obviousness over Pechanek and Dowling.

ISSUE 4

35 U.S.C. § 103(a): claims 11-14

Appellants assert their invention is not obvious over Dowling and Choquette because the combination of references do not teach the element of an "address translation memory device for accessing data at translated addresses" as recited in claim 11 (App. Br. 24-26). Appellants further contend that the recited "storage device located in the address translation memory device having data accessible at addressable locations, a second read address input internal to the address translation memory device for selecting data from the storage device during read operations, and a data output port" is not taught by Choquette (App. Br. 25 and 26, emphasis original). Specifically, Appellants argue Choquette only provides ports external to the storage device.

The Examiner maintains a "block move feature" argued by Appellants is not recited in the claims. Further, the Examiner maintains Choquette discloses a typical computer system with several parallel execution units (Ans. 14). The Examiner concludes it would have been obvious to one of ordinary skill in the art at the time of the invention to include Choquette's teaching of several read, write address and data out ports to allow for concurrent parallel processing which results in improved system throughput (*id.*).

Issue 4: Have Appellants shown the Examiner erred in finding the applied references teach an (i) "address translation memory device for accessing data at translated addresses" and (ii) "storage device located in the address translation memory device having data accessible at addressable locations, a second read address input internal to the address translation

memory device for selecting data from the storage device during read operations, and a data output port" as recited in claim 11?

FURTHER FINDINGS OF FACT (FF)

Choquette

(12) Choquette teaches a microprocessor that can process two or more program instructions simultaneously and issue program instructions to symmetrical multifunctional program execution units (Abstract).

(13) A microprocessor implementation includes two sets of three different execution units, execution unit set 14, 16, and 18 and execution unit set 20, 22, and 24 (pg. 1, [0004] and Fig. 1). The output of execution unit 14, 32a, and the output of execution unit 24, 32f, are provided to register file 30 (*id.*). The register file 30 has outputs 30a and 30b which are provided to the two sets of execution units (*id.*).

ANALYSIS

As discussed above in Issue 2, we find Dowling teaches an "address translation memory" and, since again Appellants have not provided any explicit definition, we find an "address translation memory device" is a device that includes an address translation memory. Dowling teaches a matrix multiplication function which would access data at translated addresses in performance of the multiplication and can include the elements taught in Dowling (FF 2-5 and Fig. 2). Thus, we find Dowling teaches an "address translation memory device for accessing data at translated addresses" (Fig. 2)

We next find Choquette teaches a register file, a storage unit, that has several inputs and outputs (FF 12 and 13). We agree with the Examiner that Choquette therefore discloses "a second read address input" internal to a device. Dowling teaches a storage device that has data accessible at addressable locations as set forth by the Examiner (Ans. 13 and 14). Moreover, as discussed above, the address translation memory device is not explicitly defined and thus, may include the elements taught by Dowling in Fig. 2. We thus agree with the Examiner that using multiple read address inputs within the system of Dowling to allow several execution units to execute and access the storage device in the system of Dowling would have been obvious in light of the teachings of Choquette and Dowling (Ans. 14 and 15).

As a result, we find the combination of Choquette and Dowling teaches "a storage device located in the address translation memory device having data accessible at addressable locations, a second read address input internal to the address translation memory device for selecting data from the storage device during read operations, and a data output port."

Appellants have not shown the Examiner erred in finding that the applied references disclose the disputed limitations of claim 11. Thus, Appellants have not shown that the Examiner erred in finding claim 11 is obvious over Dowling and Choquette. Claims 12-14 depend from representative independent claim 11 and were not argued separately and thus fall with claim 11.

Accordingly, Appellants have not shown the Examiner erred in rejecting claims 11-14 under 35 U.S.C. § 103(a) for obviousness over Dowling and Choquette.

ISSUE 5

35 U.S.C. § 103(a): claim 15

Appellants assert their invention is not obvious over Dowling, Choquette, and Nair for the reasons argued with respect to claims 14 and 3 reiterating that claim 14, rejected with the same rationale as claim 2, did not resolve the admitted deficiencies of Dowling and that the suggested rationale for rejecting claim 3 is not valid (App. Br. 26-27). Appellants' arguments with respect to claim 3 are that Nair merely describes operations on data elements and does not address bits nor make obvious the combinatorial logic governed by the recited equations (App. Br. 19 and 20 and claim 15, Claims Appd'x).

The Examiner argues Appellants are describing the inherent characteristics of matrix transformation; basic bitwise operation is well known in the art; and bitwise operations can be beneficially used in matrices operations (Ans. 22-24).

ANALYSIS

We agree with Appellants that the Examiner has not shown that the combination of Dowling, Choquette, and Nair teach the features of claim 15 (App. Br. 19-21 and Reply 4 and 5). Although we agree with the Examiner that Nair teaches bitwise operations, we find the Examiner has not fully explained how Nair, Choquette, and Dowling, taken alone or in combination, teach or suggest the combinatorial logic governed by the equations recited in claim 15. The gap between the explanation and the teachings and suggestion of Nair, Choquette, and Dowling is too large for us to bridge absent speculation. We will not engage in speculation. Therefore,

Appellants have shown the Examiner did not show Dowling, Choquette, and Nair teach or suggest the invention as recited in claim 15. Accordingly, Appellants have shown that claim 15 should not have been rejected under 35 U.S.C. § 103(a) for obviousness over Dowling, Choquette, and Nair.

ISSUE 6

Appellants contend that the references cited by the Examiner teach away from the present invention and that the Examiner is using hindsight to combine the references (App. Br. 27 and 28). We find these arguments unpersuasive. Appellants have presented no arguments or evidence as to why or how these references teach away from the present invention. "[A] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Kahn*, 441 F.3d 977, 990 (Fed. Cir. 2006) (quoting *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)). Nor have Appellants presented any persuasive arguments or evidence other than mere assertion as to how the combination involves hindsight. Such conclusory statements unsupported by factual evidence are entitled to little probative value. *See In re Geisler*, 116 F.3d 1465, 1470 (Fed. Cir. 1997).

DECISION

The Examiner's rejection of claims 1, 2, 4-6, 16, and 17 under 35 U.S.C. § 103(a) as being obvious over Dowling and Intel is reversed.

The Examiner's rejection of claims 3 and 19 under 35 U.S.C. § 103(a) as being obvious over Dowling, Intel, and Nair is reversed.

The Examiner's rejection of claim 18 under 35 U.S.C. § 103(a) as being obvious over Dowling and Nair is affirmed.

The Examiner's rejection of claims 7-10 under 35 U.S.C. § 103(a) as being obvious over Pechanek and Dowling is reversed.

The Examiner's rejection of claims 11-14 under 35 U.S.C. § 103(a) as being obvious over Dowling and Choquette is affirmed.

The Examiner's rejection of claim 15 under 35 U.S.C. § 103(a) as being obvious over Dowling, Choquette and Nair is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2009).

AFFIRMED-IN-PART

Vsh

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